ABSTRACT OF THE DISCLOSURE

A mesh-shaped gate electrode is located over a surface of a substrate. The mesh-shaped gate electrode includes a plurality of first elongate wirings extending parallel to one another, and a plurality of second elongate wirings extending parallel to one another. The first elongate wirings intersect the second elongate wirings to define an array of gate intersection regions over the surface of the substrate and to further define an array of source/drain regions of the substrate. To reduce gate capacitance, at least one oxide region may be located in the substrate below the mesh-shaped gate electrode. For example, an array of oxide regions may be respectively located below the array of gate intersection regions.